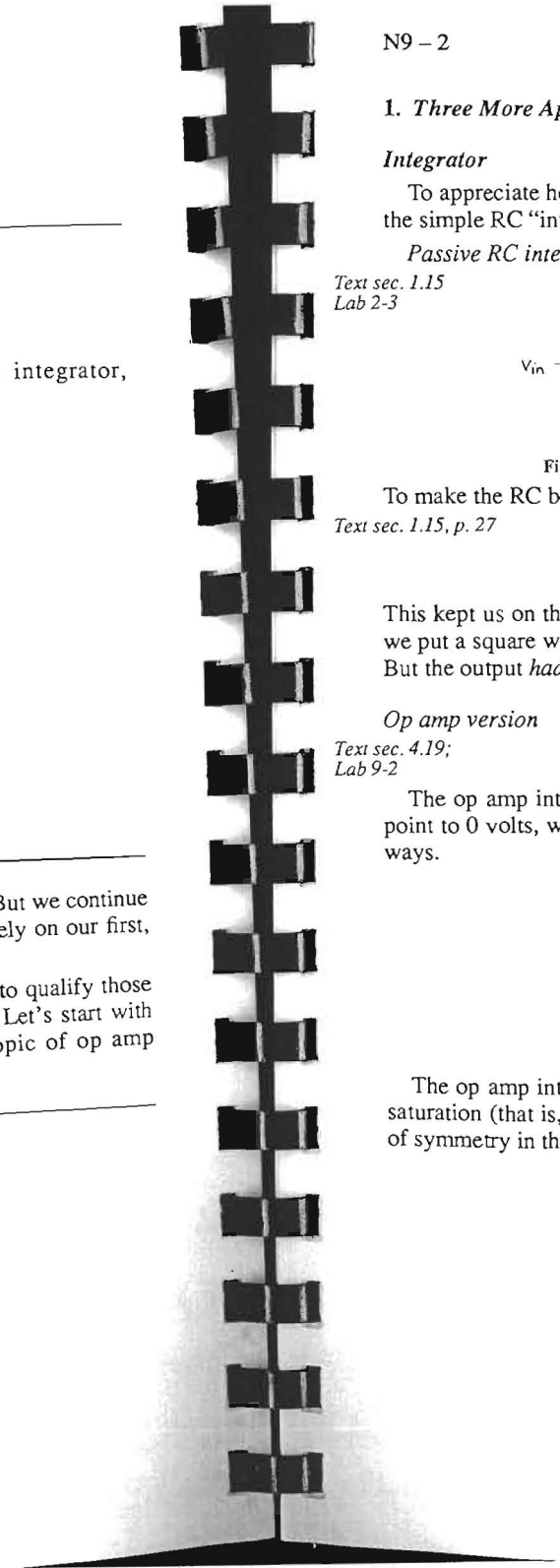
Class 9: Op Amps II: Departures from Ideal

Topics:

- *old:*
  - passive versions of circuits now built with op amps: integrator, differentiator, rectifier
- *new:*
  - three more important circuits (applications):
    - integrator
    - differentiator
    - rectifier
  - op amp departures from ideal
    - offset voltage
    - bias current
      offset current
    - frequency limitations: open-loop gain; slew rate
    - output current limit

Today we end our honeymoon with the op amp: we admit it is not ideal. But we continue to admire it: we look at more applications, and as we do, we continue to rely on our first, simplest view of op amp circuits, the view summarized in the *Golden Rules*.

After using the Golden Rules to make sense of these circuits, we begin to qualify those rules, recognizing, for example, that op amp inputs draw *a little* current. Let's start with three important new applications; then we'll move to the gloomier topic of op amp imperfections.



1. *Three More Applications:* Integrator, Differentiator, Rectifier

Integrator

To appreciate how very good an op amp integrator can be, we should recall the defects of the simple RC "integrator" you met in Chapter 1.

Passive RC integrator

Text sec. 1.15
Lab 2-3

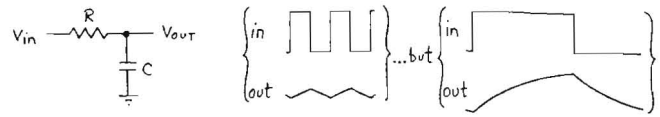


Figure N9.1: RC "integrator:" integrates, sort-of, if you feed it the right frequency

To make the RC behave like an integrator, we had to make sure that

Text sec. 1.15, p. 27

$$V_{out} \ll V_{in}$$

This kept us on the nearly-straight section of the curving exponential-charging curve, when we put a square wave in. The circuit failed to the extent that V_{out} moved away from ground. But the output *had* to move away from ground, in order to give an output signal.

Op amp version

Text sec. 4.19;
Lab 9-2

The op amp integrator solves the problem elegantly, by letting us tie the cap's charging point to 0 volts, while allowing us to get a signal out. "Virtual ground" lets us have it both ways.

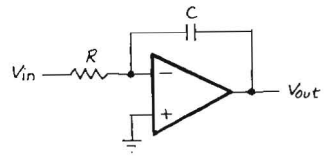


Figure N9.2: Op amp integrator: virtual ground is just what we needed

The op amp integrator is so good that one needs to prevent its output from sailing off to saturation (that is, to one of the supplies) as it integrates error signals: over time, a tiny lack of symmetry in the input waveform will accumulate; so will tiny op amp errors.

So, practical op amp integrators include some scheme to prevent the cap's charging to saturation:

*a) **One remedy: a large resistor*** in parallel with the cap (this leaks off a small current, undoing the effect of a small error current in);

p. 223

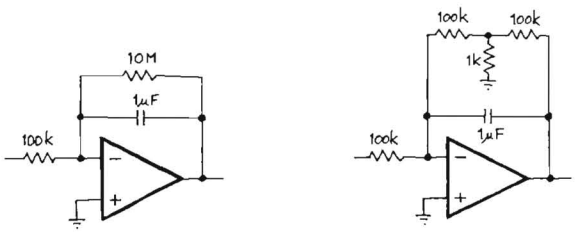


Figure N9.3: Integrator saved from saturation by resistor parallel $C_{feedback}$

Effects of the resistor

Evidently, the resistor compromises performance of the integrator. But we can figure out by *how much*. There are several alternative ways to describe its effects:

The resistor limits DC gain

In the circuit above, where R_{in} = 100k and $R_{feedback}$ = 10M, the DC gain is –100. So a DC input error of ±1 mV —> output error of ±100mV. The integrator still works fine, apart from this error.

The resistor allows a predictable DC leakage

Suppose we apply a DC input of 1V for a while; when the output reaches –1V, the error current is 1/100 the input or "signal" current (because $R_{feedback} = 100 \times R_{in}$). This error grows if V_{out} grows relative to V_{in}.

The resistor does no appreciable harm above some low frequency

At some low frequency, X_C becomes less than R, and soon R is utterly insignificant. $X_C = R$, as you know, at $f = 1/2\pi RC$. For these components—$R_{feedback}$ = 10M, C = 1μF—that frequency is about 0.01Hz!

A detail: how the resistor T works

Here's a diagram to persuade you that the clever *T* resistor arrangement does indeed make the 100k resistor look about 100X as large:

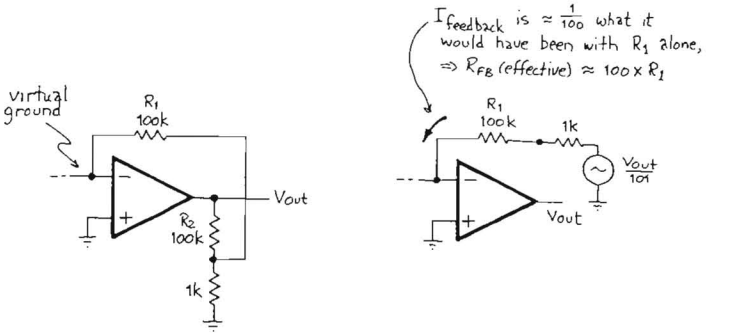


Figure N9.4: How the *T* arrangement enlarges apparent *R* values

Neat? The scheme is useful because the lower $R_{Thevenin}$ of the *T* feedback network has two good effects:

- it generates smaller I_{bias} errors than the use of giant resistors would (we'll discuss this problem, below);
- it drives stray capacitance at the op amp input better (avoiding unintentional low-pass effects in the feedback); this is not important here, but is in a circuit where no capacitor sits parallel to a big feedback resistor.

b) Another remedy: a switch in parallel with the cap (this has to be closed briefly, from time to time).

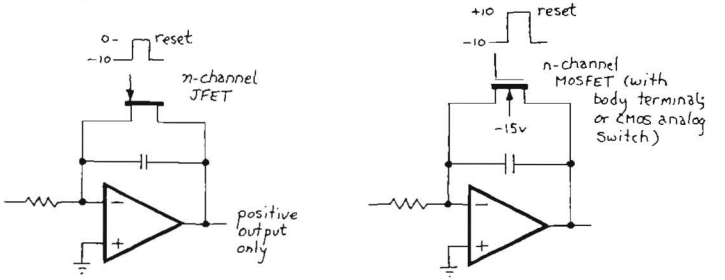


Figure N9.5: Integrator saved from saturation by discharge switch

The switch produces a more perfect integrator, but is more of a nuisance to drive.

Differentiator

ec. 4.20;
-3

Again the contrast with a passive differentiator helps one appreciate the op amp version:

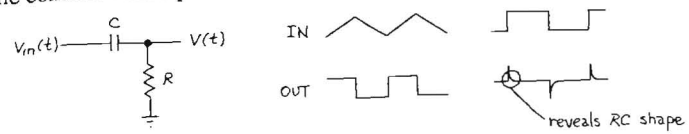


Figure N9.6: RC "differentiator:" differentiates, sort-of, if RC kept very small

To make it work, we must make sure that

sec. 1.14, p.25.

$$dV_{out}/dt \ll dV_{in}/dt$$

Again the op amp version exploits *virtual ground* to remove that restriction:

sec. 4.20,
14-25,
4.51, 4.52

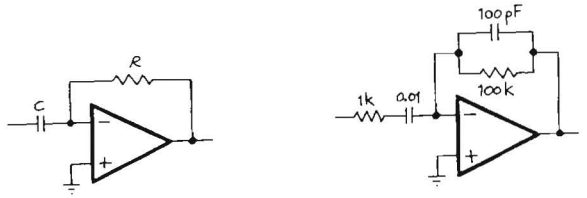


Figure N9.7: Op amp differentiator: simple (idealized); practical

This op amp differentiator is a little disappointing, however: it *must* be compromised in order to work at all. A practical differentiator, shown on the right in the figure above, turns into an integrator (of all things!) at some high frequency.
This scheme is necessary to prevent oscillations (we will look more closely at this topic a class or two hence).

Active Rectifier

xt sec. 4.10,
. 187-88, figs. 4.25, 4.26;
b 9-4

The simple passive rectifier of Chapter 1 was blind to inputs < about 0.6 v, and put an offset of that amount between input and output. The op amp version hides the diode drop:

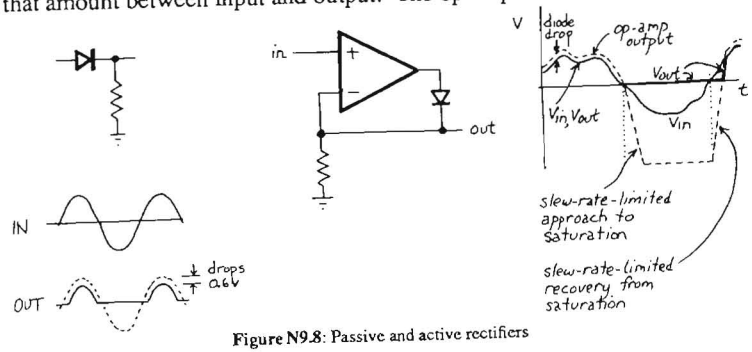


Figure N9.8: Passive and active rectifiers

The circuit shown *saturates* for one input condition. That is poor: produces an output glitch (caused by delay) as it comes up out of saturation. In the lab you will build an improved active rectifier that cleverly stays out of saturation (how does it work?)

Fig. 4.27;
Lab 9-5

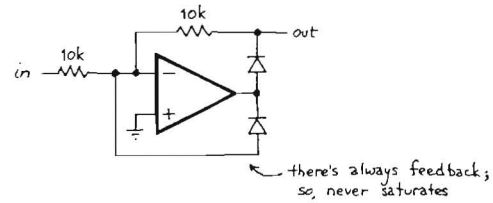


Figure N9.9: Improved active rectifier

2. Op Amp Departures from Ideal

Let's admit it: op amps aren't quite as good as we have been telling you: the Golden Rules exaggerate a bit:

- the inputs *do* draw (or squirt) a little current;
- the inputs are not held at precisely equal voltages.

Here are three circuits that always deliver a saturated output after a short time. They would not if op amps and all components were ideal:

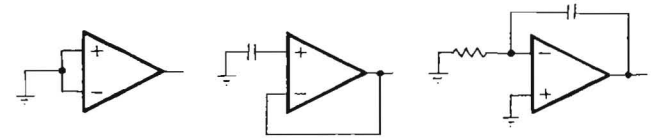


Figure N9.10: Three circuits sure to saturate. why?

Op Amp Errors

Text sec. 4.11, 4.12;
Lab 9-1

We will treat, in turn, the following op amp errors:

- *voltage offset*:
- *bias current*
  offset current
- frequency limitations: *open-loop gain roll-off; slew rate*
- *output current limit*.

Offset Voltage

Text sec, 4.11, p. 192;
4.12, p. 194

> ***Offset Voltage: V_{OS}***
> "The difference in input voltage necessary to bring the output to zero..." (Text, p. 192)

This spec describes the amp's delusion that it is seeing a voltage difference between its inputs when it is not. The amp makes this mistake because of imperfect matching between the two sides of its differential input stage.

Symbol	Parameter	Conditions	LF411A min	LF411A typ	LF411A max	LF411 min	LF411 typ	LF411 max	Units
V_{OS}	Input offset Voltage	R_S=10kΩ, T_A=25°C		0.3	0.5		0.8	2.0	mV

Figure N9.11: 411 Spec: V_{offset}

You can compensate for this mismatch by deliberately pulling more current out of one side of the input stage than out of the other, to balance things again. This correction is called 'trimming offset,' and you will do it in today's lab. But this trimming is a nuisance, and the balancing does not last: time and temperature-change throw V_{offset} off again.

The better remedies are, instead—

- use a good op amp, with low V_{offset};
- design the circuit to work well with the V_{offset} of the amp you have chosen.

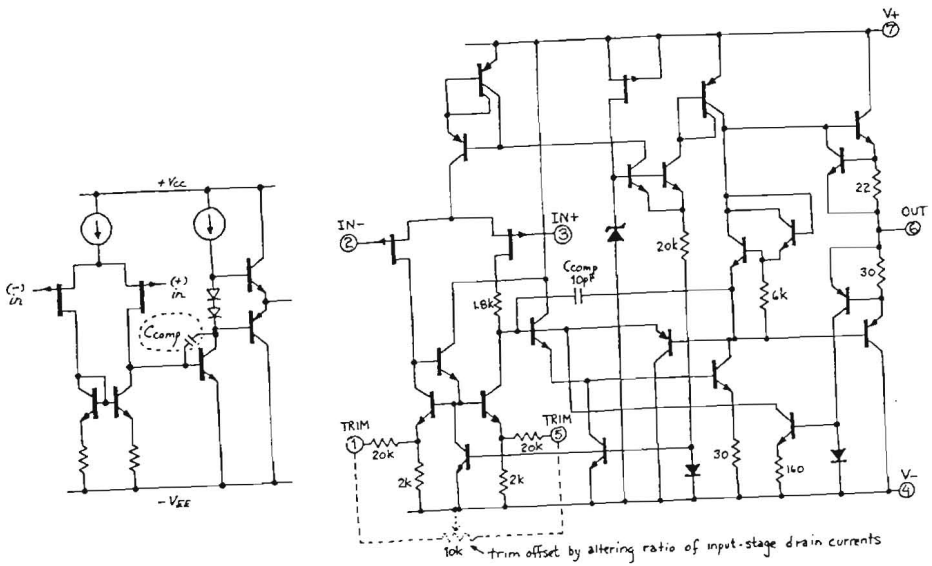


Figure N9.12: Inside the 411: schematics: simplified, and detailed

Bias Current

Text sec. 4.11, p. 190; sec. 4.12, p. 194

Symbol	Parameter	Conditions		LF411A min	LF411A typ	LF411A max	LF411 min	LF411 typ	LF411 max	Units
I_{OS}	Input Offset Current	V_S = ±15V	T_J=25°C		25	100		25	100	pA
			T_J=70°C			2			2	nA
			T_J=125°C			25			25	nA
I_B	Input Bias Current	V_S = ±15V	T_J=25°C		50	200		50	200	pA
			T_J=70°C			4			4	nA
			T_J=125°C			50			50	nA

Figure N9.13: 411 Specs: I_{bias} and I_{offset}

> ***Bias Current: I_{bias}***
>
> I_{bias} is a DC current flowing in or out at the input terminals (it is defined as the average of the currents at the two terminals).

For an amplifier with bipolar transistors at the input stage, I_{bias} is base current; for a FET-input op amp like the 411, I_{bias} is a leakage current: it is tiny, therefore, but also grows rapidly with temperature:

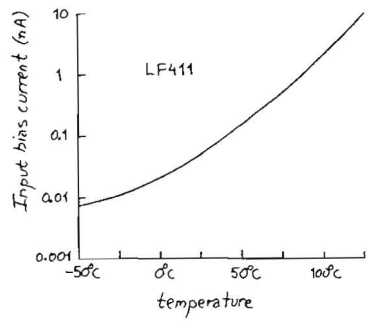


Figure N9.14: 411 bias current: tiny, but grows fast with temperature

The bias current flows through the resistive path feeding each input; it can, therefore, generate an input error voltage, which may be amplified highly to generate an appreciable output error: the Lab exercise uses a high-gain DC amplifier for just that purpose:

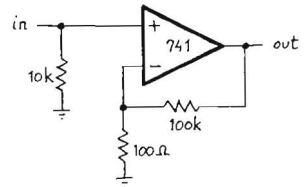


Figure N9.15: Lab circuit: uses high-gain dc amp to make errors measurable

But notice that the lab notes ask you to use a *741* op amp, not a 411, to make the errors substantial. That requirement suggests that often you will *not* need to worry about the effects of bias current: true, but you should know how to judge whether or not to worry.

To minimize the effects of bias current, match the resistances of the paths that feed the two op amp inputs. Here are examples of circuits that do or do not balance paths:

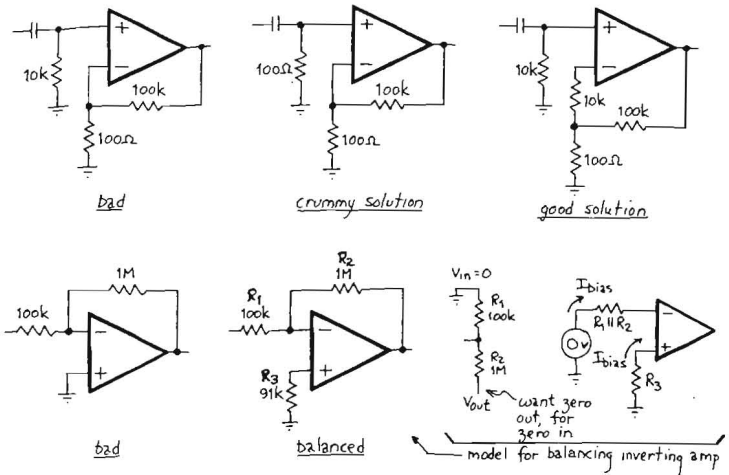


Figure N9.16: Balanced Resistive paths minimize output errors resultinG from bias current

Once you have balanced these resistive paths, I_{bias} no longer causes output errors. But a difference between currents at the inputs still does. That difference is called—

Offset Current

sec. 4.11, p. 190;
4.12, p. 195

> ***Offset Current: I_{bias}***
> The difference between the bias currents flowing at the two inputs.

For the 411 the I_{OS} specification is about 1/2 I_{bias}; for the bipolar op amps I_{OS} is smaller relative to I_{bias}. But recall how *tiny* I_{bias} is for the 411 and other FET-input devices.

As noted just above, even when the resistances seen by the two inputs are balanced, an error will occur because of this *difference* in currents. Remedy? Use resistances of moderate value. (< a few 10's of Megohms; recall the argument for the clever *T* resistor trick noted above.)

Note, by the way, that even if bias current were zero, still you would need to provide a DC connection to each op amp input, to define the voltage there; otherwise stray capacitance gradually would charge with leakage currents (in the PC board, if nowhere else). So, these two circuits are bad:

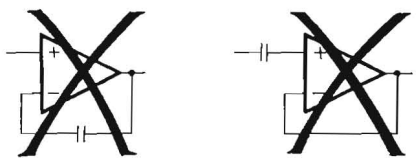


Figure N9.17: One must provide a DC connection to each op amp input

*Measuring and correcting effects of V_{offset} and I_{bias}, in lab exercise **9-1***

The lab notes suggest that you go through this process in a particular sequence. Make sure you understand why you are asked to proceed as stated there:

You start with a high-gain amp (×1000) that will show large output errors for small input errors. At the outset, the effects of V_{offset} and I_{bias} are *commingled*. You cannot tell, looking at the output, what the effect of either error is, taken by itself. Their effects may even tend to cancel.

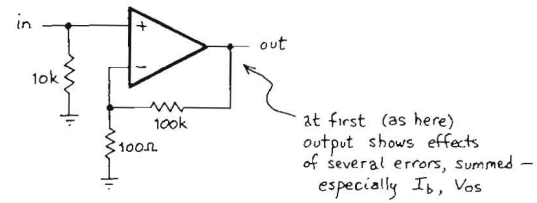


Figure N9.18: Lab 9-1's high-gain DC amp, once more

The procedure suggested goes this way:

- arrange things so that the effects of I_{bias} are negligible. (How?)
  - Measure the output error; infer the input error, and thus V_{OS}.
  - Trim V_{OS} to a minimum.
- arrange things so that I_{bias} causes an input error.
  - measure the output error so caused, and infer the input error, and thus I_{bias}.
  - Alter the circuit so as to minimize the error caused by I_{bias}
- Infer I_{OS} from the remaining output error.

Make sense?

AC Amplifier: An elegant way to minimize effects of I_{bias}, V_{OS} and I_{OS}

Text sec. 4.05,
p. 179, fig. 4.7;
Lab 10-1

If you need to amplify AC signals only, you can make the output errors caused by V_{OS} I_{bias} and I_{OS} negligible in a clever way: just cut the DC gain to unity:

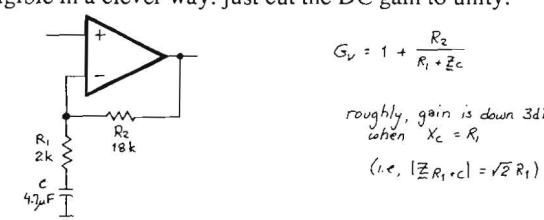


Figure N9.19: AC amplifier: neatly makes effects of small errors at *input* small at *output*

What's its f_{3dB}? If one ignores the "1" in the gain expression, output amplitude is dow 3dB when the denominator in the gain expression is $\sqrt{2}(R_1)$. But that happens when X_C R_1, and that happens, as you well know, at $f_{3dB} = 1 / (2\pi R_1 C)$.

This is the same notion you used to choose the emitter-bypassing capacitor, back in Chapter 2:

ec. 2-13, p.85

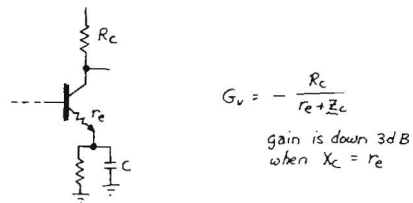


Figure N9.20: Gain is down 3dB when denominator (series impedance of R and C) is up to R√2: true for bypassed-emitter amp, and for op-amp AC amp

Slew Rate & Roll-off of Gain

sec. 4.11, pp. 191-92;
1.12, p. 193

These effects turn out to be caused, deliberately, by a gain-killing capacitor planted within the op amp. We will talk about this *compensation* device next time, when we consider op amp stability. For the moment, we will note that the op amp's gain falls off at –6dB/octave (as if the output had been passed through a simple RC low-pass: in effect, it has been!); so the chip's very high gain, necessary to make feedback fruitful, evaporates steadily with increasing frequency—and is *gone* at a few MHz (about 4 MHz for the 411).

Symbol	Parameter	Conditions	LF411 min	LF411 typ	LF411 max	Units
A_{VOL}	Large-signal voltage gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2K$, $T_A = 25°C$	25	200		V/mV
		over temperature	15	200		V/mV

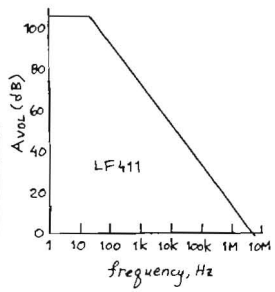


Figure N9.21: 411 gain roll-off: spec and curves

In addition, op amps misbehave in some odder ways: they think, for example, that they see a voltage difference between their inputs even when there is none.

These specifications define an upper limit on the usefulness of *all* op amp circuits; that limit explains why not every circuit should be built with op amps, wonderful though the effects of feedback are.

Output Current Limit

Text sec. 4.11, p. 191;
sec. 4.12, p. 194

This is a self-protection trick inserted into the output stage, to protect the small transistor there from the heating that otherwise would result when some clumsy user overloaded th amp. You saw a curve like this one in the first op amp lab:

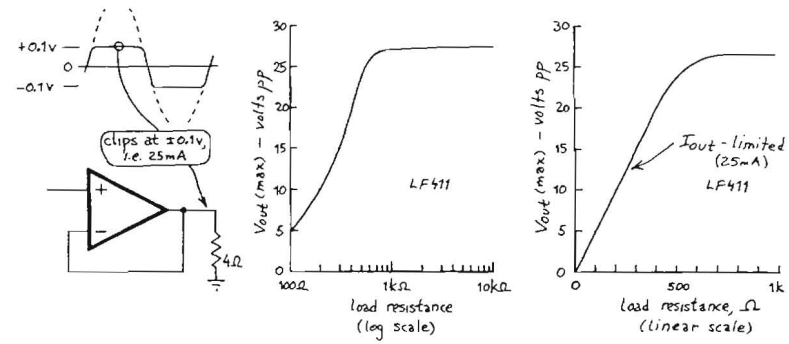


Figure N9.22: Output current limit: output clips under load, despite very low R_{out}

Ch.4: Worked Examples: Integrators; Imperfect op amps

Two worked examples:

1. Integrator design
2. Calculating effect on integrator of op amp errors

1. Integrator Design:

> ***Problem: Integrator***
>
> Design an op amp integrator that will ramp at + 1V/ms given a + 1V DC input. Include protection against drift to saturation, and let the input impedance be ≥ 10MΩ.

Solution

Let's start with a sketch, postponing the choice of part values. The *sign* of the output ramp, and the high required input impedance require a couple of extra op amps; but we don't mind: remember?: *op amps are cheap.*

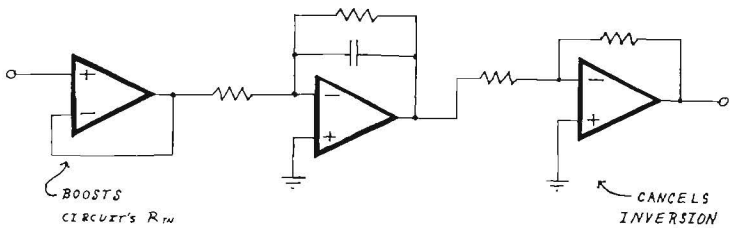


Figure X9.1: Integrator: skeleton circuit

The resistor in the feedback path will limit the DC gain, keeping the op amp output from sailing away to saturation.

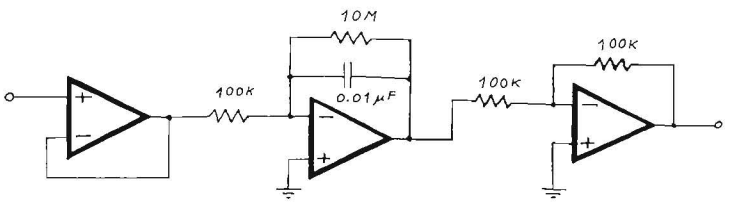
A subtle point: why not balance paths for I_{bias}

We seem to be violating our own design rules by failing to provide a resistor to ground on the non-inverting side of the integrator. Here's the argument that says it turns out better *not* to do such balancing in this context:

- we would use a low-bias-current op amp in an integrator; probably we would use an op amp with FET input and the pA currents that are usual for this type. This kind of op amp's I_{OS} will be only about a factor of two better (lower) than its I_{bias}.
- why not take that factor of two, though? Because a side effect of the large R on the non-inverting terminal is increased vulnerability to noise there. In the present case, we would use 100k at that point, whereas now the non-inverting terminal is driven by a good low impedance (ground!).

Now for part values: we want DC gain of around 100, so we don't want R_1 huge: make it, say, 100k; then $R_{feedback}$ can be about 10M.

Given R_1, we can solve for the required C using our usual description of a capacitor's behavior, $I = C\,dV/dt$. I is the current that flows when the 1V input is applied; dV/dt was given us as a design goal. We can solve for C:



$C = I / \frac{dV}{dT}$; $I = \frac{V_{IN}}{R_1}$

LET $R_1 = 100K$.

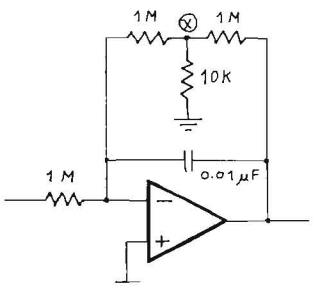
THEN $I = 0.01\,mA$ @ $V_{IN} = 1V$

$\Rightarrow C = \frac{0.01\,mA}{10^3\,V/s} = 0.01\,\mu F$

Figure X9.2: Integrator with part values specified

2. Op Amp Errors: effects on an integrator

An integrator will show the effects of even small DC errors, over time. In the next example we will try to calculate the size of those output errors.

> ***Problem: Effect on integrator of op amp errors***
>
> What output drift rate would you see in the circuit below, assuming that you use each of the listed op amps. The circuit input is grounded.
>
> $C = I / \frac{dV}{dT}$; $I = \frac{V_{IN}}{R_1}$
>
> Let $R_1 = 10K$
>
> Then $I = 0.1\,mA$
>
> $\Rightarrow C = \frac{0.1 \times 10^{-3} A}{10^3\,V/s}$ $0.1\,\mu F$
>
> 
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>
> *Figure X9.3: Integrator: what drift rates? Proposed remedy: resistor "T" feedback network*
>
> | Op amp type | V_{OS} | I_{bias} |
> |---|---|---|
> | 741C | 6mV | 500nA |
> | OP-07A | 25μV | 2nA |
> | LF411 | 2mV | 0.2nA |
>
> What happens if we add the indicated resistor network parallel to the feedback capacitor?

Solution:

The *offset voltage*, V_{OS}, causes the op amp to pull its inverting terminal (by means of the feedback network, of course) not exactly to ground, but to a voltage V_{OS} away from ground (we cannot predict the sign of this error). That error causes current to flow in the resistor; that current can't go into the op amp, so it flows into the capacitor.

The *bias current* flows into (or out of) the op amp's inverting terminal. This produces a drop across the input resistor, which must be canceled by an equal value of current flowing through the integrating capacitor (that is, it produces an output voltage *ramp*).

Worst case, these two currents flowing in the capacitor simply add. So, we get the following results:

Op amp type	V_{OS}	I_{bias}	1 <— V_{OS}	Sum of 1's	dv/dt
741C	6mV	500nA	6nA	≈ 500nA	50V/s (50mV/ms)
OP-07A	25μV	2nA	25pA	≈ 2nA	0.2 V/s
LF411	2mV	0.2nA	2nA	2.2nA	0.2 V/s

Figure X9.4: Output errors for a particular integrator made with each of three op amps

Question: "What happens if we add the indicated resistor network parallel to the feedback capacitor?"

Answer:

The Resistor network...

t sec. 4.19, 4.49, p. 223

The network looks like about 100MΩ: one part in 100 of V_{out} reaches point 'X;' so, the current flowing through the leftmost resistor is about 1/100 what it would be if that resistor alone (1M) were in the feedback path. In other words, if we apply Ohm's Law —$R_{(apparent)} = V_{out\text{-}op\text{-}amp} / I$— we find that the network behaves like a resistor of about 100M (101M, if you care).

..Its Effect

The '100MΩ' resistor gives the circuit a DC gain of –100. So, instead of sailing off to saturation, the op amp output will begin to drift at about the rate determined in the earlier section of this problem—and then will slow and finally level off at –100×(*input error voltage*).

The input error voltage is the sum of V_{OS} and I_{bias} flowing in the resistance it "sees." What is that? It's the 1M input resistor parallel the other path, which looks like 1M + 10K ≈ 1M. Parallel, the two look like 0.5MΩ:

$$V_{error(in)} = (I_{bias} \times R_{Th\text{-}bias}) + V_{OS}$$

This input error (of undetermined sign) gets amplified by –100. Here are the specific results for the three op amps.

Op amp type	V_{OS}	I_{bias}	V <— I_{bias} (I_{bias}×0.5MΩ)	Sum	Output Error
741C	6mV	500nA	0.25V	≈ –0.25V	+25V (saturation)
OP-07A	25μV	2nA	1mV	≈ 1mV	±100mV
LF411	2mV	0.2nA	0.1mV	2.1mV	≈ ±200mV

Figure X9.5: Output error (DC) for integrator with feedback resistance added

And here is a sketch of what the output voltage error would look like if we started with no charge on the cap: disaster for the '741, but tolerable results for both of the better op amps:

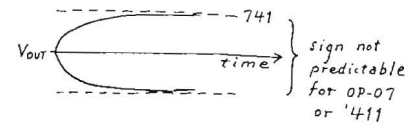

Figure X9.6: Feedback resistor limits integrator's output drift: effect quantified

Lab 9: Op Amps II

Reading:	Chapter 4.10-4.22, pp. 187-229.
Problems:	Problems in text. Additional Exercises 1-4. Bad Circuits A,C,H.

This lab introduces you to the sordid truth about op amps: *they're not as good as we said they were last time!* Sorry. But after making you confront op amp imperfections in the first exercise (9-1) we return to the cheerier task of looking at more op amp applications—where, once again, we treat the devices as ideal. On the principle that a person should eat his spinach before the mashed potatoes (or is it the other way round?) let's start by looking at the way that op amps depart from the ideal model.

9-1 Op-amp Limitations

a. Slew Rate

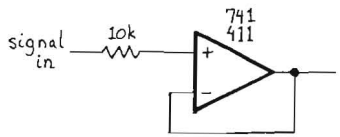

Figure L9.1: Slew rate measuring circuit. (The series resistor prevents damage if the input is driven beyond the supply voltages)

Begin by measuring slew rate and its effects, with the circuit above. We ask you to do this in two stages:

1) ***Square wave input***

Drive the input with a square wave, in the neighborhood of 1kHz, and look at the output with a scope. Measure the slew rate by observing the slope of the transitions.

Suggestions:

- Find a straight central section; avoid the regions near "saturation"—near the limits of output swing;
- Full slew rate is achieved only for strong "overdrive:" a large difference signal seen at the input of the amplifier;
- The rates for slewing up and down may differ.

See what happens as the input amplitude is varied.

2) ***Sine input***

Switch to a sine wave, and measure the frequency at which the output amplitude begins to drop, for an input level of a few volts. Is this result with the slew rate that you measured in part 1), just above?

Now go back and make the same pair of measurements (slew rate, and sine at which its effect appears) with an older op amp: a 741. The 741 claims a "typical" slew rate of 0.5V/μs; the 411 claims 15V/μs. How do these values compare with your measurements?

b. Offset Voltage

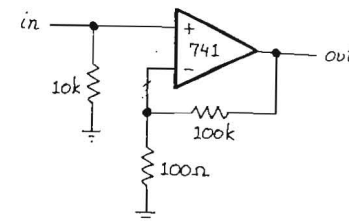

Figure L9.2: Offset measuring circuit

Now construct the ×1000 non-inverting amplifier shown above. Measure the offset voltage, using the amplifier itself to amplify the input offset to measurable levels.

Note: use a *741*, not a *411*, for the remainder of this exercise (9-1). The 411 is too *good* for this exercise: its bias current is so tiny that you would not see appreciable errors attributable to I_{bias}. (You might reasonably infer that you can forget about I_{bias}, simply by choosing a good op amp. Often you can. This exercise means to prepare you for the unusual case in which I_{bias} *does* produce troublesome errors.)

1) ***Measure*** effects of V_{offset}

The trick here, where you are to look for the effect of *offset voltage*, is to arrange things so that you can measure that effect *alone*, eliminating effects of *bias current*. To do this, you need to think what to do with the "in" terminal so as to make the effects of I_{bias} negligible. The 741's typical I_{bias} is 0.08μA (80 nA).

Compare your measured offset voltage with specs: V_{OS} = 2mV(typ), 6mV(max).

2) ***Minimize*** the effects of V_{offset}: offset trim

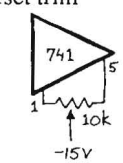

Figure L9.3: 741 offset trimming network

Trim the offset voltage to zero, using the recommended network (figure above).

c. Bias Current

Now remove the connection from "in" to ground that you should have used in part (B (either a short or a 100Ω resistor). Now the input again is connected to ground only throug a 10K resistor. Explain how this input resistor allows you to measure I_{bias}. Then compar your measurement with specs: I_{bias} = 0.08μA(typ), 0.5μA(max).

d. Offset Current

Alter the circuit in such a way that both op-amp input terminals see 10k driving resistance, yet the overall voltage gain of the circuit is unchanged. This requires some thought.

> *Hints*:
>
> - You will need to add one resistor somewhere;
> - That resistor should carry the bias current that is flowing to the inverting terminal.
> - The goal is to let the junction of the two feedback resistors sit at ground while the inverting terminal is allowed to sit below ground, at a voltage equal to that of the inverting terminal.)

Once you have done this, the effects of bias current are canceled, and only the effect of "offset current" (the difference between bias currents at the two op-amp input terminals) remains as an error. Calculate I_{os} from the residual DC level at the output; compare with specs: $I_{os} = 0.02\mu A(typ), 0.2\mu A(max)$.

Note: In the remainder of this lab except 9-4, and in all other op amp exercises, use an LF411 op amp, not the 741. In 9-4, where we ask you to use a *single-supply type*, use the '358. You will not need the 741 again.

9-2 Integrator

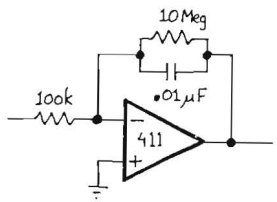

Figure L9.4: Integrator

Construct the active integrator shown above. Try driving it with a 1kHz square wave. This circuit is sensitive to small DC offsets of the input waveform (its gain at DC is 100); if the output appears to go into saturation near the 15 volt supplies, you may have to adjust the function generator's **OFFSET** control. From the component values, predict the peak-to-peak triangle wave amplitude at the output that should result from a 2V(pp), 500Hz square wave input. Then try it.

What is the function of the 10Meg resistor? What would happen if you were to remove it? Try it. Now have some fun playing around with the function generator's DC offset — the circuit will help you gain a real gut feeling for the meaning of an integral!

9-3 Differentiator

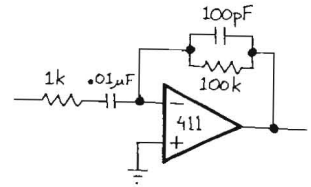

Figure L9.5: Differentiator

The circuit above is an active differentiator. Try driving it with a 1kHz triangle wave.

The differentiator is most impressive when it surprises you. It may surprise you if you apply it to a *sine* from the function generator: you might expect a clean cosine. In fact, some generators (notably the Krohn-Hite generators that we prefer in our lab) will show you a differentiated waveform that reveals the purported *sine* to be a splicing of more-or-less straight-line segments. This strange shape reflects the curious way the sine is generated: it is a triangle wave with its point whittled off by a ladder of four or five diodes. The diodes cut in at successively higher voltages, rounding it more and more as the triangle approaches its peak:

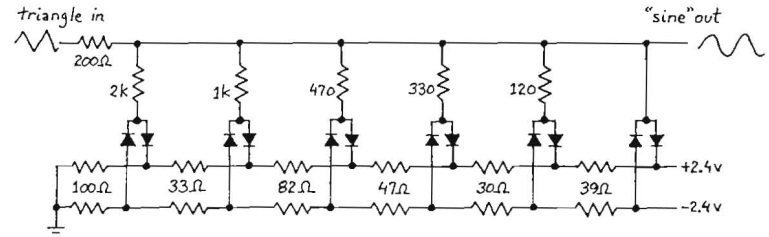

Figure L9.6: Sketch of standard function-generator technique for generating sine from triangle

You may even be able to count the diodes revealed by the output of the differentiator.

A note on stability:

Here we are obliged to mention the difficult topic of stability, a matter treated more fully in a later lab (Lab 10: op amps III). Differentiators are inherently unstable, because a true differentiator would have an overall 6dB/octave rising response; as explained in the text section 4.20, this would violate the stability criterion for feedback amplifiers. To circumvent this problem, it is traditional to include a series resistor at the input, and a parallel capacitor across the feedback resistor, converting the differentiator to an integrator at high frequencies. That is disappointing—and you may notice the effect of this network it is most evident as a deviation of phase shift, at some frequencies, from the 90° that you would expect. Incidentally, a faster op amp (one with higher f_T) would perform better: the switch-over to integrator must be made, but the faster op amp allows one to set the switchover point at a higher frequency.

9-4 AC amplifier: microphone amplifier

A. Single-supply Op Amp

In this exercise you will meet use a "single-supply" op amp, used here to allow you to run it from the +5V supply that later will power your computer. This op amp, the 358 dual (also available as a "quad" — the 324) can operate like any other op-amp, with $V_+ = +15V$, $V_- = -15V$; however, it can also be operated with $V_- = GND$, since the input operating common

mode range includes V-, and the output can swing all the way to V-. Our application here does not take advantage of the single-supply op amp's hallmark: its ability to work right down to its negative supply (ground), incidentally. Often that is the primary reason to use a single-supply device.

> **NOTE**: build this circuit on a private single breadboard strip of your own, so that you can save the circuit for later use: it will feed your computer. This is the first of three such circuits that you will build; you can put them each on a single strip, or you can build them all on a larger board.

Here the 358 is applied to amplify the output of a microphone—a signal of less than 20 mV—so as to generate output swings of a few volts. The "AC amplifier" configuration, you will notice, is convenient here: it passes the input bias voltage to the output, without amplification (gain = 1 at DC).

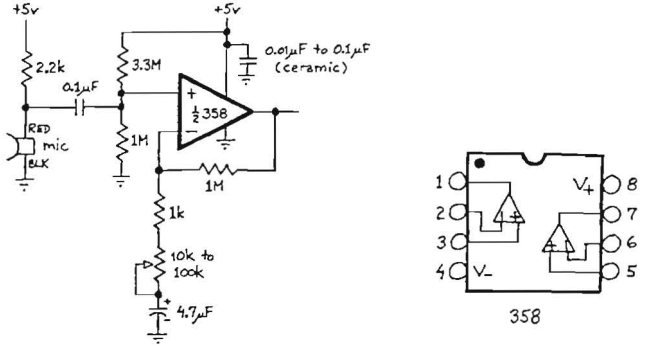

Figure L9.7: Single-supply microphone amplifier

The microphone is an "electret" type (the sound sensor is capacitive: sound pressure varies the spacing between two plates, thus capacitance; charge is held nearly constant, so V changes with sound pressure, according to $Q = CV$); it includes a FET buffer within the package. The FET's varying output current is converted to an output voltage by the 2.2k pullup resistor. So, the output impedance of the microphone is just the value of the pull-up resistor: 2.2k.

If you are troubled by oscillations on the amp output, try isolating the power supply of the microphone, thus:

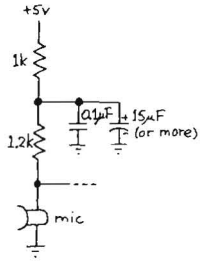

Figure L9.8: Quieting power supply to microphone

You may find, after your best efforts, that your amplifier still picks up pulses of a few tens of millivolts, at 120Hz. The pulses look like this:

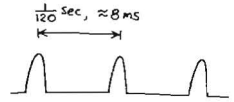

Figure L9.9: Ground noise on PB503 breadboard: caused by current pulses recharging filter capacitor

Probably you will have to live with these, unless you want to go get an external power supply (the adjustable supply you used in Lab 1 will do fine, here). These pulses show the voltage developed in the ground lines when the power supply filter capacitor is recharged by the peaks of the rectifier output. They *shouldn't* be there, but they are hard to get rid of. They appear because of a poor job of defining ground in the PB503 circuit, and you can't remedy that defect without rewiring the innards of the PB503.

9-5 Active Rectifier

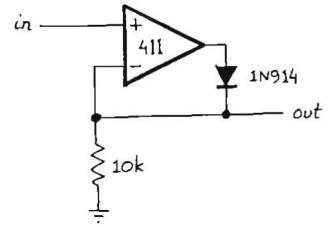

Figure L9.10: Active half-wave rectifier

Construct the active rectifier shown above. Note that the output of the circuit is not taken at the output of the op-amp. Try it with relatively slow sine waves (100Hz, say). Look closely at the output: What causes the "glitch"? Look at the op-amp output — explain. What happens at higher input frequencies?

9-6 Improved Active Rectifier

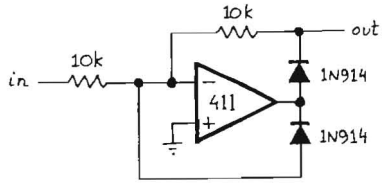

Figure L9.11: Better active half-wave rectifier

Try the clever circuit shown above. The glitch should be much diminished. Explain the improved performance. (You may want to look at the op amp output, to see the contras with the earlier case.)

9-7 Active Clamp

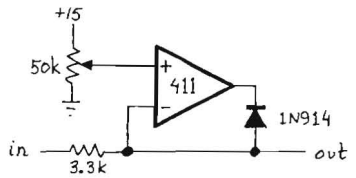

Figure L9.12: Active clamp

Try the op-amp clamp circuit shown above. (Note again that the circuit's output is not taken from the op-amp output; what significance does that have in terms of output impedance?). Drive it with sine waves at 1kHz, and observe the output. What happens at higher frequencies? Why?

Reverse the diode. What should happen?

CHAPTER 4 (continued) & CHAPTER 5

Class 10: Positive Feedback, Good and Bad: Comparators, oscillators, and unstable circuits; a quantitative view of the effects of negative feedback

Topics:

- effects of feedback: toward a quantitative view
  - feedback: generalized model
  - generalizing the effect of feedback (quantitative account)
- positive feedback:
  - comparator: fast diff amp with versatile output stage
  - hysteresis ("Schmitt trigger")
    - why hysteresis?
    - how much hysteresis?
    - how choose component values for given hysteresis? contrasted with aiming for exact threshold voltages
  - two circuits using positive *and* negative feedback:
    - rc "relaxation oscillator"—easily built from schmitt trigger
    - negative impedance converter (nic)
  - more oscillators, good and bad:
    - good oscillators
      - square wave: the *classic* 555
      - sine wave: wien bridge
    - nasty oscillators: positive feedback that sneaks up on you
      - op amp circuits:
        - why they may oscillate: funny things in the loop
        - remedies: how to prevent oscillation: 'frequency compensation'
      - oscillations without op amps: follower
        - why it oscillates
        - remedies